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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,980	01/16/2002	Takashi Kumamoto	42390P9482D	3004

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,980	KUMAMOTO ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1003*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended response filed July 28, 2003 (Certificate of Mailing date: July 24, 2003). The Examiner acknowledges the amendment of Claim 1 and the addition of new Claims 14-22. Claims 1-22 are now pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Venkateshwaran et al. (US 6,339,254 B1)* Kaminaga et al. (US 6,321,734 B1)*

Chia et al. (US 6,081,997)* Baba et al. (US 6,071,755)*

Tsukagoshi et al. (US 5,804,882)*

*Previously made of record in the instant Application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5-7, 14-18 and 22 are rejected under 35 U.S.C. 102(e) as being anticipate by Venkateshwaran et al.

As to Claim 1, Venkateshwaran et al. discloses, in Figs. 4 and 6A: a chip 401 comprising a top surface (i.e., the active surface having bumps 411), a bottom surface (opposite the top surface) and side surfaces disposed between the top and bottom surfaces; a substrate 610 comprising an upper surface; a plurality of reflowed solder bumps 411 (col.6: 36-43) electrically coupling the top surface with an adjacent portion of the upper surface; a monolithic element comprising solidified resin 410 (col.4: 47-48 and col.6: 16-18); the monolithic element encapsulating and adhesively bonded to (i) substantially all the side surfaces of chip 401, (ii) a substantial portion of the upper surface (of substrate 610), and (iii) the plurality of reflowed bumps 411 located in a gap between the top surface of chip 401 and the upper surface of substrate 610 (col.4: 28-34 and 41-43). The limitation "the monolithic element resulting from a single molding process" is a process limitation in a product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art in the case that the product is the same as, or obvious over, the prior art (in the present case, Venkateshwaran et al.). See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

As to Claim 2, Venkateshwaran et al. further discloses that the solidified resin does not encapsulate the bottom (exposed) surface of chip 401 (Fig. 4).

As to Claim 3, Venkateshwaran et al. discloses that resin 410 further comprises a filler material (col.4: 28-34 and 41-43).

As to Claim 5, Venkateshwaran et al. further discloses that resin 410 encapsulates substantially all of the side surfaces of chip 401 (Fig. 4).

As to Claim 6, Venkateshwaran et al. further discloses that the solidified resin does not encapsulate the bottom (exposed) surface of chip 401 (Fig. 4).

As to Claim 7, Venkateshwaran et al. further discloses that the solidified resin comprises an epoxy (col.2: 53-58, col.4: 47-48 and col.6: 16-18).

As to Claim 14, the limitation "wherein the resin was injected into a mold surrounding the chip and the substrate" is a process limitation in a product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art in the case that the product is the same as, or obvious over, the prior art (in the present case, Venkateshwaran et al.). See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

As to Claim 15, Venkateshwaran et al. discloses, in Figs. 4 and 6A: a substrate 610 comprising a first (upper) surface; a chip 401 comprising a first surface (i.e., the active surface having bumps 411), a second surface (opposite the first surface) and one or more edges, the first surface of chip 401 being coupled with the first surface of substrate 610 by a plurality of solder bumps 411 (col.6: 36-43) providing electrical connection between chip 401 and substrate 610; a solid resin element 410 (col.4: 47-48 and col.6: 16-18), the solid resin element 410 encapsulating and bonding to the first surface of chip 401, all the edges of chip 401, the first surface of substrate 610 and the

plurality of solder bumps 411 (col.4: 28-34 and 41-43). The limitation "the solid resin element resulting from a process of injecting liquid resin into a mold containing the chip and the substrate" is a process limitation in a product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art in the case that the product is the same as, or obvious over, the prior art, (in the present case, Venkateshwaran et al.). See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

As to Claim 16, the solid resin element 410 is not bonded with the second (i.e., exposed) surface of chip 401 (Fig. 4).

As to Claim 17, the limitation "wherein the second surface of the chip was in contact with the mold during the process of injecting liquid resin into the mold" is a process limitation in a product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art in the case that the product is the same as, or obvious over, the prior art, (in the present case, Venkateshwaran et al.). See Product-by-Process in MPEP § 2113 and 2173.05(p) and *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).

As to Claim 18, Venkateshwaran et al. discloses that resin 410 further comprises a filler material (col.4: 28-34 and 41-43).

As to Claim 22, Venkateshwaran et al. further discloses that the solidified resin comprises an epoxy (col.2: 53-58, col.4: 47-51 and col.6: 16-18).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkateshwaran et al. in view of Chia et al. and Kaminaga et al.

I. Venkateshwaran et al. discloses that resin 410 further comprises a filler material including electrically insulating and thermally conductive particles and having a low thermal coefficient of expansion (TCE) for the purpose of: (i) lowering the thermal coefficient of expansion (TCE) of the resin 410 in order to alleviate the TCE mismatch problems that adversely affect the integrity and reliability of the solder bump connections, and (ii) provide thermally conductive particles for dissipating heat from the chip surfaces (col.4: 28-34, 41-43 and 47-51). However, Venkateshwaran et al. is silent as to the composition, shape and size of the filler material.

II. Chia et al., in the same packaging art as Venkateshwaran et al., discloses silica particles in a solidified resin encapsulant 32 that are electrically insulating and thermally conductive for the same purpose as that of Venkateshwaran et al. (Fig. 3; col.6: 40-51) but is silent as to the shape and size of the particles.

III. Kaminaga et al., in the same packaging art as Venkateshwaran et al. and Chia et al., teaches silica spherical particles for reducing the TCE of resin encapsulant 4

(as in Venkateshwaran et al. and Chia et al), preventing discrete packaging parts and the substrate from being damaged by sharp particle edges and further teaches that it is preferable that the spherical particles be very small, i.e., "microspheres" in order to enhance the fluidity of the resin encapsulant, thereby ensuring that the resin completely encapsulates the chip and its bumps in the transfer mold (Fig. 3; col.5: 48-51; col.7: 3-28 and 61-65; col.10: 66-col.11: 3).

IV. Since Venkateshwaran et al., Chia et al. and Kaminaga et al. are all in the same packaging art and are solving similar TCE mismatch problems and heat dissipation problems, then the use of silica particles (Chia et al.) that are very small spheres, i.e., microspheres (Kaminaga et al.) would have been readily recognized for all the above-cited benefits taught by Chia et al. and Kaminaga et al., respectively, in the pertinent art of Venkateshwaran et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the low TCE, heat dissipative filler material particles of Venkateshwaran et al. with the silica microspheres taught by Chia et al. and Kaminaga et al. in order to ensure the reliability of the resin-encapsulated package of Venkateshwaran et al. with all the above-cited enhancements, as taught by Chia et al. and Kaminaga et al.

7. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkateshwaran et al. in view of Chia et al. and Kaminaga et al., as applied to Claims 19 and 20 above, and further in view of Tsukagoshi et al.

I. Venkateshwaran et al., as modified by Chia et al. and Kaminaga et al. teaches microspheres comprised of silica (see col.5: 48-51, col.7: 3-28 and 61-65, and col.10: 66-col.11: 3 of Kaminaga et al.) but does not teach microspheres comprised of glass.

II. Tsukagoshi et al. discloses an epoxy resin underfill 11 (col.7: 16-26) used to bond chip 1 to substrate 4, the epoxy resin 11 comprising micron-sized insulating filler particles (col.7: 53-62 and col.8: 42-48), wherein these micron-sized insulating filler particles can be spherical and made of silica or glass, among other materials which are recognized equivalents for performing the functions of fillers in epoxy resin underfills (col.8: 49-55).

III. Since Tsukagoshi et al. and Venkateshwaran et al., as modified by Chia et al. and Kaminaga et al. are in the same art of assembling electronic packages using epoxy resin underfills with microspherical silica fillers, the use of the equivalent microspherical glass fillers taught by Tsukagoshi et al. would have been readily recognized in the pertinent art of modified Venkateshwaran et al. to perform the same functions of the microspherical silica fillers in the epoxy resin underfill of modified Venkateshwaran et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art to replace the microspherical silica fillers of modified Venkateshwaran et al. with the equivalent microspherical glass fillers, as taught in Tsukagoshi et al., for the purpose of controlling package reliability factors, such as the resin underfill viscosity and/or the thermal expansion mismatch problems between the packaging elements, recognized and solved by the use of the equivalent microspherical silica fillers in modified Venkateshwaran et al., said replacement of silica microspherical fillers with glass

microspherical fillers (taught as equivalents by Tsukagoshi et al.) being influenced by matters of cost and package reliability relating to the types of materials being used in the various elements of the package (e.g., substrate materials, composition of solder balls, etc.) of modified Venkateshwaran et al. in which the epoxy resin with the microspherical fillers is being used as the underfill.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkateshwaran et al. in view of Baba et al.

I. Venkateshwaran et al. discloses that the package 400 of Fig. 4 has an embodiment wherein substrate 610 is a multilayer substrate (col.5: 41-47) but is silent as to the thickness dimension of the substrate.

II. Baba et al. discloses, in Fig. 17, a multilayer substrate 34 having insulating layers 37 and wiring layers 36, wherein the insulating layers are polymer materials (e.g., epoxy, polyimide) with no reinforcing fibers (a so-called "neat" substrate) which enables the substrate 34 to be thin so that the package profile can be minimized in accordance with the industry trend towards miniaturization of multi-functionality electronic devices (col.1: 9-14; col.11: 11-25).

III. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the multilayer substrate 610 of Venkateshwaran et al. with the multilayer substrate structure of Baba et al. in order to obtain a thin substrate for the purpose of enabling the electronic package of Venkateshwaran et al. to have a reduced profile in keeping with the industry trend towards package

miniaturization of multi-functional devices desirable in the market place for electronics, as taught by Baba et al.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkateshwaran et al. in view of Baba et al., as applied to Claim 8 above, and further in view of Applicant's admitted prior art.

I. Modified Venkateshwaran et al. discloses all the limitations of the claim including the modification of the multilayer substrate 610 of Venkateshwaran et al. with the "neat" polymer substrate of Baba et al. in order to obtain a thin substrate for miniaturizing the package, wherein the modification further includes that the "neat" insulating layer 37 may be "several tens to several μm" which enables the entire substrate 34 to be thin (Baba et al., Fig. 17 and col.11: 22-25) which has the added benefit of improving the electrical performance of the resulting package (col.11: 38-30). Note that although "no through holes are provided" in the substrate, there are short blind vias through each of polymer layers 37 that connect the wiring layers 36 (as can be seen in each of the polymer layers 37 of substrate 34 of Fig. 17) which include the disclosed power/ground layers (col.11: 28-30), wherein the vias through the neat polymer layers 37 are inherently shorter between the wiring layers 36 they connect because the neat polymer layers 37 are made thinner which inherently shortens the vias and improves the electrical performance by reducing the length of the wiring paths which reduces parasitic line inductance effects.

II. However, Venkateshwaran et al. thus modified by Baba et al. does not teach that the "neat" polymer multilayer substrate is specifically in the thickness range of approximately 0.05 mm (i.e., 50 μm) to 0.5 mm (i.e., 500 μm) thick.

III. Applicant's admitted prior art also teaches that in prior art packaging "[i]t is desirable in many integrated circuit applications to utilize as thin a substrate or film as possible to maximize the electrical performance of the resulting packaged chip" and furthermore that "[t]ypically, thin substrates or films are comprised of a polymeric material and are 0.05 to 0.5 mm thick," wherein the "thin substrates shorter vias help reduce loop inductance within the substrate." (Applicant's Specification, p.4, paragraph [0006]: lines 1-5).

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the substrate of Venkateshwaran et al., as modified by Baba et al., by arranging the multilayer substrate of modified Venkateshwaran et al. such that the neat polymer layers 37 having the thickness dimensions of "several tens to several μm," as taught by Baba et al., are set at a thickness and are employed in the number of layers so that the total thickness of substrate 34 meets the typical prior art standard for thin substrates of approximately 0.05 mm (i.e., 50 μm) to 0.5 mm (i.e., 500 μm) thick, as taught in Applicant's admitted prior art, in order for the substrate of Venkateshwaran et al., as modified by Baba et al, to be useful in a wide variety of known electronics applications.

10. Claims 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkateshwaran et al. in view of Baba et al.

A) As to Claim 9:

I. Venkateshwaran et al. discloses that the package 400 of Figs. 4 and 6A has an embodiment wherein substrate 610 is a multilayer substrate (col.5: 41-47) but is silent as to the material of the substrate.

II. Baba et al. discloses, in Fig. 17, a multilayer substrate 34 having insulating layers 37 and wiring layers 36, wherein the insulating layers are polymer materials (e.g., epoxy, polyimide) with no reinforcing fibers (a so-called "neat" substrate) which enables the substrate 34 to be thin so that the package profile can be minimized in accordance with the industry trend towards miniaturization of multi-functionality electronic devices (col.1: 9-14; col.11: 11-25).

III. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the multilayer substrate 610 of Venkateshwaran et al. with the "neat" polymer material for the insulating layers of the multilayer substrate structure, as taught by Baba et al. in order to obtain a thin substrate for the purpose of enabling the electronic package of Venkateshwaran et al. to have a reduced profile in keeping with the industry trend towards package miniaturization of multi-functional devices desirable in the market place for electronics, as taught by Baba et al.

B) As to Claim 11:

I. Venkateshwaran et al. discloses, in Figs. 4 and 6A, all the limitations of the claim including an additional chip 402 electrically coupled with substrate 610 but does not teach at least one passive component electrically coupled with substrate 610.

II. Baba et al. discloses, in Fig. 20, a capacitor 53 coupled to substrate 34 along with chips 31 (col.12: 31-35), typically functioning as a noise decoupling capacitor for suppressing noise on the power line and preventing such noise spikes from reaching the power contacts of chip 31 and adversely affecting the performance of the chip.

III. Since Venkateshwaran et al. teaches encapsulating more than one chip 401 in Figs. 4 and 6A, and since the problem of power line noise solved by Baba et al. would have been readily recognized in the pertinent art of Venkateshwaran et al., then it would have been obvious to one of ordinary skill in the art at the time the invention was made to either replace additional chip 402 with, or add to encapsulated substrate 610, a decoupling capacitor, as taught in Baba et al., in order to provide a noise decoupling capacitor at least for chip 401, as in Baba et al., thereby improving the performance of the package 400 of Venkateshwaran et al.

C) As to Claim 12, modified Venkateshwaran et al. further discloses that the solidified resin 410 inherently fills a gap between a first surface (i.e., the lower non-contact surface) of the capacitor, elevated above substrate 610 by the conductive joining material (as taught in modifier reference Baba et al., Fig. 20: see capacitor 53 mounted on substrate 34) and an adjacent surface of the substrate 610.

D) As to Claim 13, modified Venkateshwaran et al. further discloses that the solidified resin 410 fully encapsulates the capacitor (as in Fig. 20 of modifier reference Baba et al.) that replaces the chip 402 of modified Venkateshwaran et al.

Response to Arguments

11. Applicant's arguments filed in the instant Amendment of July 28, 2003 have been fully considered but they are not persuasive. The Applicant has amended base Claim 1 by inserting a product-by-process limitation therein and provided a similar product-by-process limitation in new base Claim 15. Also, new dependent Claims 14 and 17 are product-by-process claims. The Applicant argues, in the case of base Claim 1, and implies, in the case of new base Claim 15, that the insertion of the respective product-by-process limitations into these base claims renders the claims patentable over the prior art of record. The Examiner respectfully disagrees and fully addresses this issue in the rejections of base Claims 1 and 15, as well as in the rejections of dependent Claims 14 and 17, above.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Odashima et al. (US 5,998,243; *already made of record in Applicant's IDS filed October 06, 2003 as Paper No. 1003*) discloses (col.6: 1-25) a solidified resin 24 (Figs. 2C and 3) resulting from a single-step process of injecting liquid resin 23 into a mold 8 containing the chip 12 and the substrate 13 (Fig. 2B).

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Primary Examiner
Art Unit 2827

jbv
November 11, 2003